Routing Technologies for 28 nm and Beyond

Increased design sizes, multiple goals, and DRC/DFM complexity and are creating a raft of significant routing challenges.

As the IC industry accelerates adoption of the 32/28 nm process node, designers are facing significant new challenges with digital routing. These challenges—including complex design rule checking (DRC) and design for manufacturing (DFM) rules, increasing rule counts, very large (1 billion transistor) designs, and multiple optimization objectives—impede the ability of design teams to meet quality, time-to-market, and cost targets. For 28 nm and below, designers must adopt new routing technologies that can solve for multiple design objectives within the scope of required tool capacity, memory footprint, and runtime.

NANOMETER ROUTING CHALLENGES

The primary challenges at 28 nm that require new routing technologies include:

- Growing number of DRC/DFM rules and rule complexity
- Poor global routing estimations
- Disconnected physical signoff and engineering change order (ECO) iterations

GROWING DRC/DFM REQUIREMENTS

Design rules and DFM requirements exist to correct for the parametric, systematic, and random manufacturing defects that occur when trying to print features smaller than the wavelength of light used in the lithography process. Integrated device manufacturers (IDMs) and foundries have roughly doubled the required design rules between the 90 nm and 28 nm nodes to ensure layout features known to affect yield are not introduced into the design (Figure 1). In addition, model-based DFM analysis is being used to detect more subtle yield limiters, and is becoming mandatory. All of these factors essentially make designers more responsible for ensuring that a design not only meets functional and performance specifications, but is also manufacturable.

For 28 nm, foundries provide “recommended rules” in addition to the mandatory DRC rules. Recommended rules are soft rules that improve the yield and each comes with a priority that reflects its relative impact on manufacturability. Although recommended rules are discretionary, if they are not honored during implementation, they can have a direct impact on yield.

POOR GLOBAL ROUTING ESTIMATION

Before creating detailed routes, routing tools perform a ‘global routing’ step which estimates the available routing resources. It is very important for these global routing estimates to be accurate, which means more than simply counting the number of routing tracks across the chip that meet minimum spacing requirements. The estimate must take into account complex resource requirements such as the effect of vias and stacked via arrays, blockages, and staggered macros. It must also consider design rule compliance and SI requirements like wire spreading, wire widening, and shielding.

Some routing engines use only a subset of the foundry design rules in a simplified form for global routing, and invoke the full set of DRC rules only for detail, or final routing. The result is poor correlation between early estimates and final routing results and ultimately, routing closure problems.

DISCONNECTED PHYSICAL SIGNOFF AND ECO ITERATIONS

Another key challenge seen at 28 nm is a result of the traditional decoupling of the routing and the signoff verification engines. Typically, a router uses simplified DRC and DFM models to provide the optimal trade-off between runtime and accuracy during routing. Once the implementation is complete, the GDSII layout is verified using signoff-quality DRC/DFM models and Standard Verification Rule Format (SVRF) rule decks. For previous nodes, this worked adequately because the number of violations discovered at signoff was relatively low. However, at advanced nodes, there can be a huge number of DRC/
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DFM violations, and changes made to fix them can lead to new manufacturing violations, or negatively impact the performance targets of the design.

Additionally, there is a growing difference between the rules used during design and those in the signoff rule deck. As a new process node matures, the foundry’s design rule files, expressed in the SVRF language used by sign-off engines, are constantly updated to address manufacturing issues as they are discovered. Consequently, these foundry signoff models are intrinsically the most accurate and complete representation of actual manufacturing requirements. The rules used by the place and route system, expressed in LEF or similar syntax, are simpler and frequently fall out of sync with the foundry rules. Further, at 28 nm and below, there are some rules that simply cannot be expressed in the simpler LEF language. As a result, the router will report the layout to be DRC/DFM, but signoff analysis finds a large number of violations.

Designers are also finding that DFM techniques, including metal fill/CMP, litho, and critical area analysis, are starting to affect the traditional design metrics like timing, power, and signal integrity. These challenges are made worse by the fact that there is no automated way to repair the DRC/DFM violations, and the traditional flow requires the transfer of huge ASCII files between the implementation and signoff environments, which slows the design process. In summary, the design-then-verify flow that has worked in the past is increasingly unmanageable and unpredictable.

CAN THE ROUTER HANDLE 28 NM?

Routers employed in 28 nm IC designs need to be flexible and robust. Modern routers should support both gridded and non-gridded models and use a universal connectivity model for a friendly ECO flow. It should also support sophisticated non-default rules (NDRs) and all the DFM requirements for advanced nodes including recommended rules, redundant vias, wire spreading and widening, and timing-aware metal and via fill. Finally, because of the large size of many 28 nm ICs and SoCs, routers need to use multiple cores and CPUs and physical memory very efficiently. The requirements of a routing system for 28 nm are illustrated in Figure 2.

ENSURING 28 NM DRC / DFM RULES SUPPORT

The routing engines should support all the complex design rules as defined by the foundries at 32 nm and 28 nm. The

<table>
<thead>
<tr>
<th>Rule</th>
<th>130nm</th>
<th>90nm</th>
<th>65nm</th>
<th>45nm</th>
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<td>4-5</td>
<td>5-6</td>
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<tr>
<td>Min-Step (OPC)</td>
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<td>All Layers (critical)</td>
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<td>-</td>
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</table>

Figure 1. Foundries are requiring ever more design rules with each process node to ensure manufacturability. The increased number and complexity of design rules poses a challenge to signal routing.
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The router should be able to address the increased number and complexity of DRC rules by intelligently minimizing the number of operation performed during routing, thereby minimizing the impact on runtime. The algorithms should make use of the full DRC/DFM models during all stages of routing which results in improved accuracy and minimum violations during post-route optimization and signoff. The DRC engine should check for DRC rules based on polygon shapes rather than edge-to-edge checks which enable complex 28 nm rules to be represented and adhered to effectively.

In addition to the default hard rules, the router should also support recommended, or soft, rules and corresponding rule priorities. Automatic routing repair should be performed based on the priority as defined by the foundry or the user to ensure the best DFM score.

**ACCURATE RESOURCE ESTIMATION IN GLOBAL ROUTING**

For the best resource estimations, a timing- and congestion-aware 3D global router is essential to determine the routing layer resources. The global router should also use the complete set of DRC/DFM rules, including recommended rules, to avoid intractable DFM problems that typically are found as late-stage surprises. If a router cannot accurately measure the resources used by vias or stacked via patterns, it will make inaccurate congestion estimates. To improve this capability at advanced nodes, a router should use new modeling technologies that ensure that the resources consumed by vias or stacked via patterns are accounted for when calculating resource availability.

**VARIABILITY-DRIVEN ROUTING FOR TIMING, SI, POWER**

Variability must be accounted for at all levels of design at 28 nm. To ensure optimization of all design parameters across all process and operational modes and corners, the router should be multi-mode, multi-corner (MCM) aware. It must also include SI as an inherent cost function to achieve the best QoR and faster convergence. When the routing engines (global, track, and final) are driven by dynamic native SI analysis it allows for faster design closure.

Traditional routers use static SI models and proxy models, instead of native analysis, which can be slower and less accurate than what designers need. Newer routers do better by having SI costing native to the routing kernel, which allows for dynamic, incremental, MCM SI analysis. Using incremental, on-the-fly extraction, polygon-based DRC analysis, and MCM timing analysis lets a router make quick decisions on issues such as increased spacing, wire spreading, and rerouting for critical nets.

**INTEGRATED DRC AND DFM SIGNOFF**

Advanced IC designs require a fundamental change in the physical design flow, which require the physical signoff engines to be directly invoked from the place and route environment. This integrated flow requires a new flexible architecture that allows the router to natively perform SVRF-based DRC and DFM analysis. This system can ensure that all manufacturability issues are addressed without introducing new ones, and without degrading the performance of the design. This flow significantly speeds up the manufacturing signoff process, and delivers higher quality results with faster time to market.

Enabling access to the actual signoff engines running golden SVRF rule decks is the key to the effectiveness of the platform. With this approach there are no new rule languages, tools, or methodologies to learn. There are also other advantages, like on-demand GDSII abstraction, which allows designers to find LVS and DRC problems that are caused by mismatches between GDSII and abstract views.

**HIGH CAPACITY AND FAST TURN-AROUND-TIME**

Today’s routers should have an extremely efficient and scalable data model to address the growing design sizes at smaller nodes. When assessing performance, consider that
the number of operations the router must perform at 28 nm is nearly four times more than what was required at the 65 nm node. To maintain the routing runtime for these big designs several techniques can be used. One is a method for clustering and filtering rules. Rather than applying each rule separately, a more intelligent tool can detect rule commonalities and group them for more efficient processing.

Another important performance factor is the efficient use of multiple CPUs. Figure 3 illustrates the speedup that can be achieved for different CPU configurations when the P&R architecture has a very efficient data model and is built for maximum parallelism.

Advanced process node designs face a raft of significant routing challenges due to the increased number and complexity of DRC/DFM requirements, increased design sizes, and multiple design goals. Routers for 28 nm must offer a flexible and powerful architecture to address these concerns and achieve optimal QoR across all design metrics in the shortest time.

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